JP INFOTECH

2017 - 2018 VLSI IEEE FINAL YEAR Projects @ JP iNFOTeCH

S.NO	Project Code	IEEE 2017-18 VLSI Project Titles	Lang/Year
		LOW POWER	
1	JPV1701	A 2.5-ps Bin Size and 6.7-ps Resolution FPGA Time-to-Digital Converter Based on Delay Wrapping and Averaging	VLSI/2017
2	JPV1702	Coordinate Rotation-Based Low Complexity K-Means Clustering Architecture	VLSI/2017
3	JPV1703	Low-Power Scan-Based Built-In Self-Test Based on Weighted Pseudorandom Test Pattern Generation and Reseeding	VLSI/2017
4	JPV1704	A Way-Filtering-Based Dynamic Logical–Associative Cache Architecture for Low-Energy Consumption	VLSI/2017
5	JPV1705	Resource-Efficient SRAM-based Ternary Content Addressable Memory	VLSI/2017
6	JPV1706	Write-Amount-Aware Management Policies for STT-RAM Caches	VLSI/2017
7	JPV1707	Fault Diagnosis Schemes for Low-Energy Block Cipher Midori Benchmarked on FPGA	VLSI/2017
8	JPV1708	High-Throughput and Energy-Efficient Belief Propagation Polar Code Decoder	VLSI/2017
9	JPV1709	High-Speed Parallel LFSR Architectures Based on Improved State-Space Transformations	VLSI/2017
10	JPV1710	Scalable Approach for Power Droop Reduction During Scan-Based Logic BIST	VLSI/2017
11	JPV1711	Stochastic Implementation and Analysis of Dynamical Systems Similar to the Logistic Map	VLSI/2017
12	JPV1712	Efficient Designs of Multi-ported Memory on FPGA	VLSI/2017
13	JPV1713	High-Speed and Low-Latency ECC Processor Implementation Over GF(2m) on FPGA	VLSI/2017
14	JPV1714	An On-Chip Monitoring Circuit for Signal-Integrity Analysis of 8-Gb/s Chip-to-Chip Interfaces With Source-Synchronous Clock	VLSI/2017
15	JPV1715	A 2.4–3.6-GHz Wideband Sub-harmonically Injection-Locked PLL with Adaptive Injection Timing Alignment Technique	VLSI/2017
16	JPV1716	Hardware-Efficient Built-In Redundancy Analysis for Memory With Various Spares	VLSI/2017

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Pondicherry Office: JP INFOTECH, #37, Kamaraj Salai, Thattanchavady, Puducherry -9.Landmark: Near to Muruga Theatre.

17	JPV1717	Fast Automatic Frequency Calibrator Using an Adaptive Frequency Search Algorithm	VLSI/2017
18	JPV1718	A High-Efficiency 6.78-MHz Full Active Rectifier with Adaptive Time Delay Control for Wireless Power Transmission	VLSI/2017
19	JPV1719	Scalable Device Array for Statistical Characterization of BTI-Related Parameters	VLSI/2017
AREA EFFICIENT/ TIMING & DELAY REDUCTION			
20	JPV1720	VLSI Design of 64bit × 64bit High Performance Multiplier with Redundant Binary Encoding	VLSI/2017
21	JPV1721	ENFIRE: A Spatio-Temporal Fine-Grained Reconfigurable Hardware	VLSI/2017
22	JPV1722	Hybrid Hardware/Software Floating-Point Implementations for Optimized Area and Throughput Tradeoffs	VLSI/2017
23	JPV1723	Efficient Soft Cancelation Decoder Architectures for Polar Codes	VLSI/2017
24	JPV1724	Low-Complexity Digit-Serial Multiplier Over GF(2m) Based on Efficient Toeplitz Block Toeplitz Matrix–Vector Product Decomposition	VLSI/2017
25	JPV1725	Sign-Magnitude Encoding for Efficient VLSI Realization of Decimal Multiplication	VLSI/2017
26	JPV1726	FPGA Realization of Low Register Systolic All-One-Polynomial Multipliers over GF (2m) and Their Applications in Trinomial Multipliers	VLSI/2017
27	JPV1727	Low-Complexity Transformed Encoder Architectures for Quasi-Cyclic Non-binary LDPC Codes Over Subfields	VLSI/2017
28	JPV1728	Antiwear Leveling Design for SSDs With Hybrid ECC Capability	VLSI/2017
29	JPV1729	Energy-Efficient VLSI Realization of Binary64 Division with Redundant Number Systems	VLSI/2017
Audio, Image and Video Processing			
30	JPV1730	A Dual-Clock VLSI Design of H.265 Sample Adaptive Offset Estimation for 8k Ultra-HD TV Encoding	VLSI/2017
31	JPV1731	RoBA Multiplier: A Rounding-Based Approximate Multiplier for High-Speed yet Energy-Efficient Digital Signal Processing	VLSI/2017
32	JPV1732	Energy-Efficient Reduce-and-Rank Using Input-Adaptive Approximations	VLSI/2017
33	JPV1733	Dual-Quality 4:2 Compressors for Utilizing in Dynamic Accuracy Configurable Multipliers	VLSI/2017
34	JPV1734	An FPGA-Based Hardware Accelerator for Traffic Sign Detection	VLSI/2017

35	JPV1735	Soft Error Rate Reduction of Combinational Circuits Using Gate Sizing in the Presence of Process Variations	VLSI/2017
36	JPV1736	Time-Encoded Values for Highly Efficient Stochastic Circuits	VLSI/2017
37	JPV1737	Design of Power and Area Efficient Approximate Multipliers	VLSI/2017
		VERIFICATION	
38	JPV1738	COMEDI: Combinatorial Election of Diagnostic Vectors From Detection Test Sets for Logic Circuits	VLSI/2017
39	JPV1739	Reordering Tests for Efficient Fail Data Collection and Tester Time Reduction	VLSI/2017
		NETWORKING	
40	JPV1740	Multicast-Aware High-Performance Wireless Network-on-Chip Architectures	VLSI/2017
		VLSI - BACK END PROJECT - TANNER(nm) / HSPICE(nm) / DSCH3 - MICROWIND(um)	
41	JPV1741	Temporarily Fine-Grained Sleep Technique for Near- and Sub-threshold Parallel Architectures	VLSI/2017
42	JPV1742	Low-Power Design for a Digit-Serial Polynomial Basis Finite Field Multiplier Using Factoring Technique	VLSI/2017
43	JPV1743	10T SRAM Using Half-VDD Precharge and Row-Wise Dynamically Powered Read Port for Low Switching Power and Ultralow RBL Leakage	VLSI/2017
44	JPV1744	Delay Analysis for Current Mode Threshold Logic Gate Designs	VLSI/2017
45	JPV1745	Area and Energy-Efficient Complementary Dual-Modular Redundancy Dynamic Memory for Space Applications	VLSI/2017
46	JPV1746	Probability-Driven Multi-bit Flip-Flop Integration With Clock Gating	VLSI/2017
47	JPV1747	A High-Speed and Power-Efficient Voltage Level Shifter for Dual-Supply Applications	VLSI/2017
48	JPV1748	A 0.1–2-GHz Quadrature Correction Loop for Digital Multiphase Clock Generation Circuits in 130-nm CMOS	VLSI/2017
49	JPV1749	Conditional-Boosting Flip-Flop for Near-Threshold Voltage Application	VLSI/2017
50	JPV1750	An All-MOSFET Sub-1-V Voltage Reference With a–51-dB PSR up to 60 MHz	VLSI/2017
51	JPV1751	A 65-nm CMOS Constant Current Source with Reduced PVT Variation	VLSI/2017

52	JPV1752	A Fault Tolerance Technique for Combinational Circuits Based on Selective-Transistor Redundancy	VLSI/2017
53	JPV1753	Preweighted Linearized VCO Analog-to-Digital Converter	VLSI/2017
54	JPV1754	A 100-mA, 99.11% Current Efficiency, 2-mVppRipple Digitally Controlled LDO with Active Ripple Suppression	VLSI/2017
55	JPV1755	Sense Amplifier Half-Buffer (SAHB): A Low-Power High-Performance Asynchronous Logic QDI Cell Template	VLSI/2017
56	JPV1756	On Micro-architectural Mechanisms for Cache Wear out Reduction	VLSI/2017
57	JPV1757	Energy-Efficient TCAM Search Engine Design Using Priority-Decision in Memory Technology	VLSI/2017
58	JPV1758	A 92-dB DR, 24.3-mW, 1.25-MHz BW Sigma–Delta Modulator Using Dynamically Biased Op Amp Sharing	VLSI/2017
59	JPV1759	A 0.45 V 147–375 nW ECG Compression Processor With Wavelet Shrinkage and Adaptive Temporal Decimation Architectures	VLSI/2017

PROJECT SUPPORT TO REGISTERED STUDENTS:

1) IEEE Base paper.

2) Abstract Document.

3) Future Enhancement (based on Requirement).

4) Modified Title / Modified Abstract (based on Requirement).

5) Complete Source Code/Simulation File/ Hardware Kit.

6) How to Run execution help file.

7) Software Packages

8) International Conference / International Journal Publication based on your project.

OUR OTHER SALIENT FEATURES:

- Number 1 Project Master in Pondicherry/Puducherry & Chennai.
- Guided more than 30,000 students.

JP INFOTECH

- Successfully conducted more than 25 International Conferences in all over South India from 2013 to 2017.
- For the academic year **2017- 2018**, we have Signed MoU with Many Engineering Colleges in all over India to Conduct International Conferences in academic year 2017 – 2018, Where the Registered Students of JP INFOTECH, can easily publish their Project Papers.
- Published more than 3000 Research Articles of Our Ph.D./M.Phil/ME/M.Tech./BE/B.Tech. Students in Leading International Conferences and International Journals from 2013 to 2017.
- From the year **2013 to 2017,** we are Recognized and Awarded from the following colleges: "Paavai College of Engg", "Arjun College of Technology", "K.S.R. College of Engineering", "Vetri Vinayaha College Of Engineering And Technology", "SKR Engineering College", "Sree Sastha Institute of Engineering and Technology", "Jaya Engineering College", "V.P.Muthaiah Pillai Meenakshi Ammal Engineering College for Women", "Muthayammal Arts and Science College", "Sri Raaja Raajan College of Engineering and Technology", "Latha Mathavan Engineering College", "Dr Pauls Engineering College", "Jain College of Engineering", "Manakula Vinayagar Institute of Technology", "CK College of Engineering & Technology" etc.
- Recognized and published article about JP INFOTECH and its director in "THE HINDU", "DINAKARAN" and many more newspapers and Media.
- Leaders with more than 8+ years of experience
- We assist and guarantee you to publish a paper on your project in INTERNATIONAL JOURNAL PUBLICATIONS / INTERNATIONAL CONFERENCE PUBLICATIONS.
- We provide REVIEW DOCUMENTS AND PPTS for each review
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- VALID TRAINEE CERTIFICATION (ISO Certification)
- 100% PLACEMENT SUPPORT
- Own Projects are also welcomed.

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